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# DC-DC POWER CONVERTERS WITH MULTIPLE OUTPUTS

A Thesis

Submitted to the Faculty

of

Purdue University

by

Bharath Kumar Sabbarapu

In Partial Fulfillment of the

Requirements for the Degree

of

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I would like to dedicate my thesis

To my parents:

Sabbarapu Sreenu and Uma Maheshwari

for their unconditional love.

To my academic advisor:

Dr. Euzeli Cipriano Dos Santos

and

To my friend:

Omar Nezamuddin

for their immense support.

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# ABSTRACT

Bharath Kumar, Sabbarapu. M.S.E.C.E., Purdue University, August 2016. DC-DC Power Converters With Multiple Outputs. Major Professor: Euzeli dos Santos Jr.

This study presents a novel converter configuration that is related to the area DC-DC power converters. To begin with, a brief introduction is given by stating the importance of power electronics. Different types of converters, their operating principles and several new topologies that are being proposed over the years, to suit a particular application with specific advantages are listed in detail. In addition, procedure for performing small signal analysis, which is one among the several averaging techniques is summarized in the first chapter.

In the second chapter, small signal modeling is carried out on the single input dual output DC-DC buck converter [1]. This analysis is performed to get a clear understanding on the dynamics of this novel configuration [2]. Routh stability criterion is also applied on this converter topology to determine the limiting conditions for operating the converter in its stability.

Third chapter proposes the single input multiple output DC-DC synchronous buck converter [3]. It's operation, implementation and design are studied in detail. In further, small signal analysis is performed on this topology to determine the transfer function.

In the following chapter, results obtained on comparison of a losses between the conventional and traditional topologies are presented in detail. In addition, results achieved during the analysis performed in the previous chapter are displayed.

In the end, advantages and its highlights of this novel configuration proposed in this study is summarized. Future course of actions to be done, in bringing this configuration in to practice are discussed as well.

# 1. INTRODUCTION

## 1.1 Background

Fossil fuel has been a fountain head in the field of power generation [4]. As this primary fuel is being depleted over the years, search for alternate fuels grew, which lead to the rise of renewable energy systems. Due to the increase in industrial and consumer appliances, distribution of this power generated by various sources is a challenging task. This laid path to the field of Power Electronics.

Power Electronics help in controlling the flow of electrical energy between the supply and the load, offering optimized results by consuming minimum energy, longevity of equipment, meager maintenance and better controllability [5]. The concepts of power electronics in conjunction with various power processing equipments has paved for the development of several new technologies, in such a way that it optimally suits the respective application in a robust manner for convenient utilization.

The systems and machines around us, depend highly on power electronics for delivering power effectively and efficiently. Power electronics is used not only to deliver the power, but they serve us in an innumerable ways in our day-to-day life. This paved the way for the emergence of Power Converters. The major intention of a converter is that they play most pivotal role in transforming the different types of electricity for convenient use at the receiving end. They are not only used for the conversion of energy, but they are also used for conserving the energy enough to transmit the electricity over longer distances with minimum losses. The block diagram in Fig. 1.1 has been taken from [6], describes the role of power electronic converters in the renewable energy systems.

From Fig. 1.1, it can be described as, power electronic converter constitutes components, circuits and systems [7]. Where components are the basic building blocks,

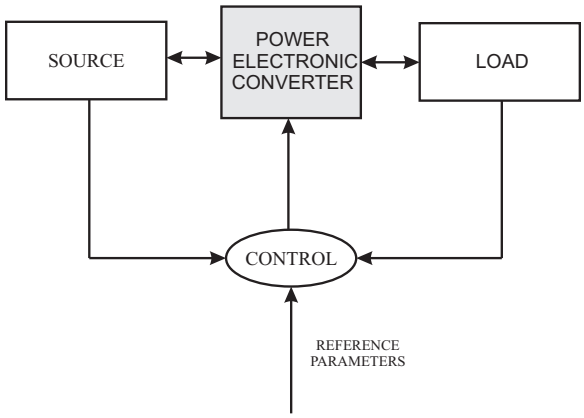



Fig. 1.1. Role of power electronic converters in the power systems

which include the semiconductor devices. Circuits and their topologies, include all the combinations consisting of these components. Systems are designed in such a way that, their integration and control has higher precedence over the electronic technology in order to obtain better power processing.

Developments in the field of power electronic converters did not come into lime light recently, but dates back to the history, the power switching devices were built on the basis of gas and vacuum [5]. These were used in the field of machine electronics as they were used to control the electro mechanical energy conversion process in the electrical machine. Subsequent advancements in technology, the power switches were devised based on the semiconductor theory [5]. Accordingly, over the years the power devices have undergone enormous changes, starting from the bi-polar power transistors, power thyristors, MOS (Metal-Oxide Semiconductor) based devices such as MOSFET (Metal-Oxide Semiconductor Field Effect Transistor) and IGBT (Insulated-Gate Bipolar Transistor). These improvements in conjunction with IC technologies [8], helped in the development of CMOS (Complimentary Metal-Oxide Semiconductor) devices. These CMOS devices along with the control circuits and high voltage transistors, led to the development of HVIC (High Voltage Integrated Circuits), which find applications in power supplies and speed drives. Thus evolved the field of Power Electronics.

These converters can be devised with several topologies with or without the conversion stages. Accordingly, a direct converter [9] is one which converts without requiring any intermediate stages. On the other hand, if a converter makes use of intermediate stages for conversion process then it is known as indirect converter [9]. While considering the indirect converters, a buffer stage is also needed to be included; if the transfer of energy is between two current sources, a capacitor is used and if it is done in between two voltage sources, an inductor is used in the buffer stage. Classification of these types of conversions will be studied in detail in the following section.

## 1.2 Classification of Power Electronic Converters based on Conversion

### 1.2.1 AC-DC Power converters

Advancements in the battery industry lead to the rise of DC products [10]. As the power supplied to the consumer terminals is of alternating in nature, charging the batteries in these DC products requires an AC to DC conversion, which is achieved by an AC-DC power converter. Different topologies are proposed in [10], where regulated DC power is generated through two power factor correctors and a switch. The resultant DC voltage is stepped down to required level by means of a DC-DC buck converter to match the load characteristics. In example [11], the proposed converter comprises of a bridge rectifier with a power factor corrector, where the output voltage is regulated by a feedback path. On the whole, bridge rectifier acts as a pivotal component in an AC-DC converter, which processes AC variables and delivers the DC variables.

### 1.2.2 DC-AC Power Converters

DC voltage is produced by the renewable energy systems, micro grid systems and energy storage systems. Since consumer distribution schema requires an AC voltage at its input terminals, a conversion from DC to AC at the generation end is required.

The DC-AC power converters operate in such a way that, it processes DC voltage supplied to its input terminals and generates a variable voltage at a variable frequency. In example [12], AC power is obtained through a bi-directional DC-DC converter and a conventional DC-AC power converter. This conversion can also be achieved by using active clamp circuits. In [13], non-complimentary active clamp circuits were used. These active clamp circuits absorb leakage energy and thereby reduces the harmonics present in voltage.

### 1.2.3 AC-AC Power Converter

As per the requirement of an appliance, AC-AC converters regulate the voltage and frequency of the AC mains. Depending upon the type of conversion required, these converters are classified into matrix [14, 15], indirect [16, 17], and direct converters [18–22]. Direct AC-AC converters are the common converter configuration used for regulating the AC voltage. Remaining other configurations which are left out, were used to regulate both the AC voltage and frequency [23]. Their merits and demerits are stated in the [23]. In another example [24], a buck boost AC-AC converter was proposed which utilizes a single bi-directional switch. In this case, efficiency of the proposed topology depends on the duty cycle of the deployed switch.

### 1.2.4 DC-DC Power Converter

The DC-DC converters are utilized for DC voltage regulation. DC-DC converters are extensively used in battery charging/discharging units [25,26], UPS [27,28], SMPS, and renewable energy systems [29]. They are operated in such a way that the required output voltage is the average of the voltage developed across the switch during its ON and OFF position. Hence, these converters either step down or step up the DC-voltage. Converters which steps down the voltage or steps up the current are known as buck converters shown in Fig. 1.2 (a).

On the other hand, converters which steps up the voltage or step down the current are called boost converters. Conventional buck and boost topologies are shown in the following Fig. 1.2 (b).

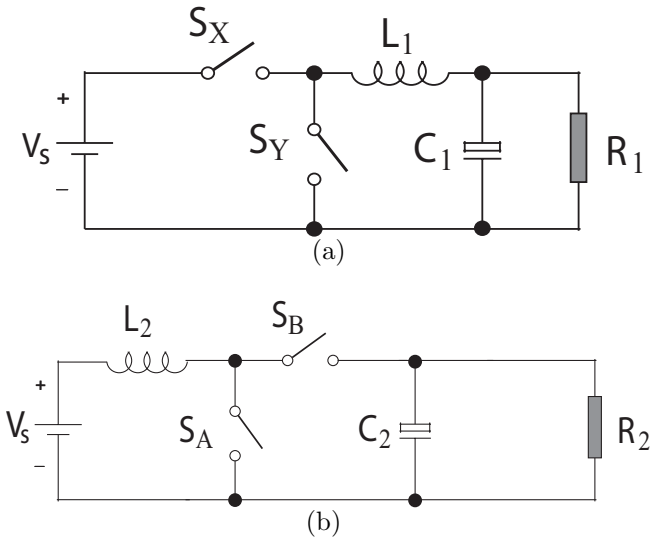



Fig. 1.2. Traditional DC-DC Converter: (a) Buck converter, (b) Boost converter.

Apart from the above, several buck boost topologies are also being proposed. In [30], proposed buck boost converter operates in buck mode under certain limits. But if arises an overload condition, converter automatically shifts to boost mode which is designed specifically for aeronautical applications. In [31], isolated buck boost converter topology is proposed. In addition to the buck and boost mode, it operates in fly back mode and possess various advantages viz. higher efficiency, power density and component utilization. Following Fig. 1.3 describes the circuit configuration of conventional buck boost DC-DC converter.

From the Fig. 1.2 and 1.3, operation of the basic components present in converters can be described as follows, switches present in all these topologies are utilized for generation of average voltage. Since this average voltage wave form consisted a ripple content. Hence in order to eliminate an LC filter is introduced.

Furthermore, DC-DC converters can be of uni-directional [32] as well as bi-directional in nature. Uni-directional single input single output DC-DC buck converter consists

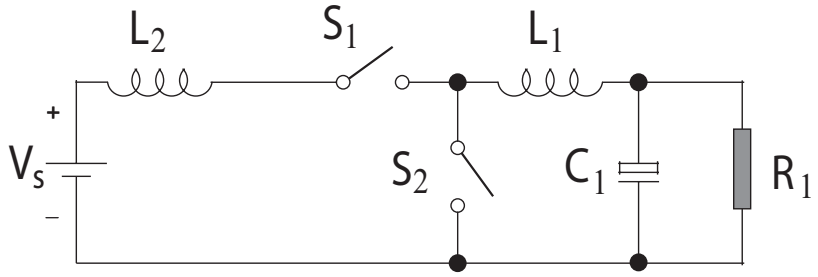



Fig. 1.3. Conventional DC-DC buck boost topology.

of single switch and a diode [2]. In order to realize a converter with bidirectional characteristics [2, 33], a diode is replaced by another switch which is operated complimentary to the switch connected in series with the power supply.

### 1.3 Classification of DC-DC Converters based on Connection

Isolated type converters provide a separation required between the high voltage sources and the sink. They are extensively used in distributive power systems, micro grid systems, renewable energy systems and uninterrupted power supply [34, 35]. However while considering the efficiency, their performance gets narrowed down since the transformers are under operation whenever the switch is either in ON (or) OFF condition. In [36], a single switch isolated DC-DC converter is proposed with following advantages: higher voltage regulation ratio and minimum number of switches compared to the conventional half bridge or full bridge configurations. Traditional isolated configuration is shown in the Fig. 1.4 below.

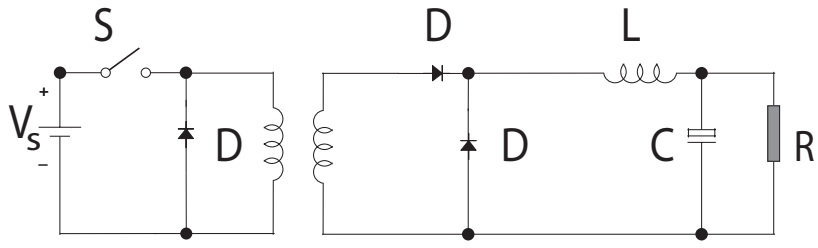



Fig. 1.4. Traditional isolated buck converter

On the other hand, non-isolated converters are efficient. They either contain an auto transformer or do not include any transformer part in the converter topology. They are popularly used in applications such as hybrid vehicles, switch mode power supplies (SMPS) and in battery charging and discharging units [37–39]. In [40], three types of transformer-less boost converters are designed which are cost effective, smaller in size and with minimum conduction losses.

Fig. 1.4 depicts the circuit connection of an isolated DC-DC buck converter, where the input and output terminals are magnetically linked. It can also observed that number of power electronic components utilized in the isolated buck converter is greater than the non-isolated buck converter whose topology is shown in Fig. 1.2 (a). In view of less number of components utilized in non-isolated buck converter, they are more efficient and cost effective.

## 1.4 Small Signal Analysis

After designing a novel configuration, it is necessary to determine the relationship between the input, output and its control variables [37]. Analysis by this method of averaging provides an efficient way of determining the above mentioned electrical dynamics of the converter [41]. Procedure for the method of performing this analysis [42, 43] is discussed as follows:

- For a particular period, state space equations are derived for every topological state observed due to the switching action.
- Each set of state space equations are multiplied by their respective duty cycles and cumulatively attain the overall state space equation of the converter.
- Laplace transformation is applied to these state space equations. There by further calculations can be done using algebra.
- Transfer function is derived where the output variables are described as a function of input and control variables.

Conditions for the analysis to be valid are briefly discussed in [41]. In [43], small signal analysis was carried out on a DC-DC boost converter for designing controllers. The equations derived for every operating state are proved by observing the voltage dynamics obtained through simulating in MATLAB/SIMULINK.

Dual output DC-DC buck converter proposed in [2] will be introduced and small signal analysis on that particular configuration [3] will be briefly explained in the following chapter. Chapter 3 deals with the same converter configuration designed for generating triple outputs [1] and it's analysis will be discussed in detail. At the end, experimental results will be depicted and future extensions will be discussed in chapters 4 and 5 respectively.

# 2. SMALL SIGNAL ANALYSIS OF SINGLE INPUT DUAL OUTPUT DC-DC BUCK CONVERTER

## 2.1 Introduction

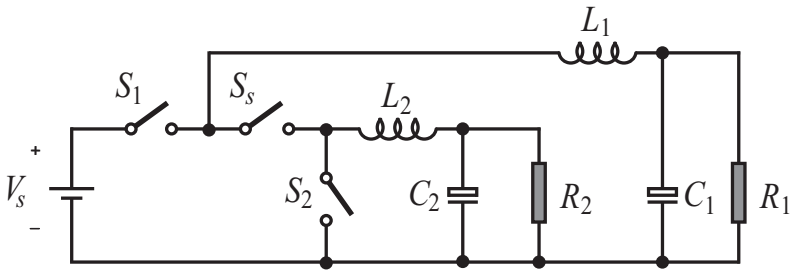
Many circuit configurations are being proposed in the area of DC-DC buck converters to meet the demands of different applications. Few among the various demands include the converter to have bi-directional characteristics, reduction in costs and better power loss distribution among the switches. These necessities are fulfilled by a converter topology proposed in [2], as shown in Fig. 2.1 (a). Fig. 2.1 (b) depicts the traditional circuitry for a DC-DC converter with a single input and dual output converter.

To implement this novel configuration for the real time applications, parameters that govern the performance of the power electronic converters are to be considered. Which includes it's transient response and its voltage regulation [44]. In order to control these variables we approach towards area of control theory [45]. This theory, focuses upon designing the controllers for the converter, in return making the system to have a feedback path. Since the primary objective of the converter is to deliver a constant output voltage, closed loop systems should be designed in such a way that any change in the input voltage or the load current should not affect the output voltage. Several averaging and linearization techniques that can be implemented on the DC-DC converter topologies are briefly discussed in [41].

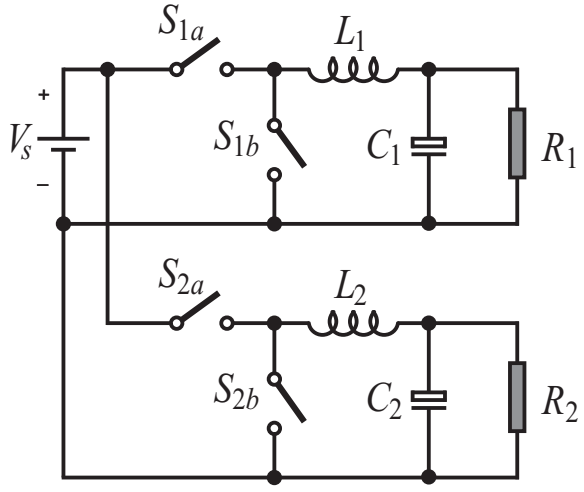
Small signal modeling is one among those techniques that help in deriving the relations between the input, control and output variables. For this analysis to be applied on the converter topologies few conditions are to be satisfied, which are discussed in [41]. Small signal modeling is applied on multi resonant and quasi resonant converters [46], AC/DC power factor correction unit [44], Half bridge complimentary

control DC-DC converter [47]. Which is primarily used to determine functions such as the open loop frequency response, control to output and input to output transfer functions. Since these conditions are met by the converter topology proposed in [2], small signal analysis is applied on this topology, and expressions are derived among the output variables and the control variables, Where the control variables could be supply voltage and duty cycle of the switches $S_1$, $S_2$ and $S_s$.

This chapter provides a detailed analysis on single input dual output converter topology by deriving the transfer functions. In addition, simulation results are presented where the converter modeling is validated by comparing the simulation in time and frequency domains.




(a)




(b)

Fig. 2.1. Single input dual output DC-DC buck converter: (a) Proposed topology, (b) Traditional topology.

## 2.2 Small Signal Analysis

As stated in [2], their operational states are shown in the Fig. 2.2 for the reference. Let us assume $D_x$, $D_y$, $D_z$ be the respective duty cycles for each topological state. This means that for one period, topological state 1 is under operation for a time period of $T_{on-x}$. Similarly topological states TS-2 and TS-3 will remain for a period of $T_{on-y}$ and $T_{on-z}$ respectively.

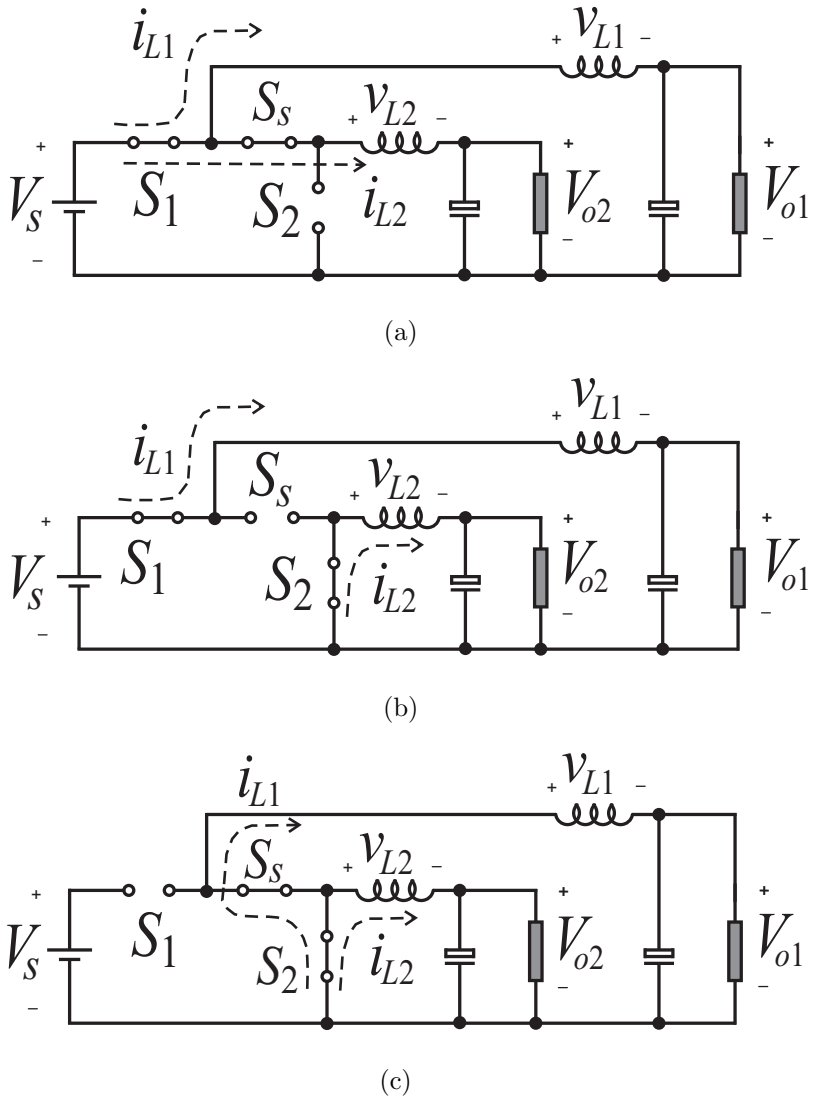



Fig. 2.2. Single input dual output DC-DC buck converter's: (a) Topological state 1 (TS-1), (b) Topological state 2 (TS-2), (c) Topological state 3 (TS-3).

In order to control the output voltage, we express these duty cycles in terms of switching duty cycles. Hence the obtained relations are listed below:

$$D_x + D_y = D_1 \tag{2.1}$$

$$D_x + D_z = D_s \tag{2.2}$$

$$D_z + D_y = D_2 \tag{2.3}$$

$$D_z = 1 - D_1 \tag{2.4}$$

$$D_y = 1 - D_s \tag{2.5}$$

$$D_x = 1 - D_2 \tag{2.6}$$

Where $D_1$, $D_2$ and $D_S$ are the duty cycles of the switches $S_1$, $S_2$ and $S_s$ respectively. In order to derive a relation between the input and the output variables, transfer functions are calculated using state space average method as followed in [43], [48]. Kirchoff's voltage and current law's are applied to the topological states TS-1, TS-2 and TS-3 and thereby obtained equations are written below:

Topological state-1:

$$L_1\frac{di_{L1}}{dt} + V_{01} = V_s \tag{2.7}$$

$$L_2\frac{di_{L2}}{dt} + V_{02} = V_s \tag{2.8}$$

$$C_1\frac{dV_{01}}{dt} + \frac{V_{01}}{R_1} = i_{L1} \tag{2.9}$$

$$C_2\frac{dV_{02}}{dt} + \frac{V_{02}}{R_2} = i_{L2} \tag{2.10}$$

Topological state-2:

$$L_1\frac{di_{L1}}{dt} + V_{01} = V_s \tag{2.11}$$

$$L_2\frac{di_{L2}}{dt} + V_{02} = 0 \tag{2.12}$$

$$C_1\frac{dV_{01}}{dt} + \frac{V_{01}}{R_1} = i_{L1} \tag{2.13}$$

$$\frac{V_{02}}{R_2} - C_2\frac{dV_{02}}{dt} = i_{L2} \tag{2.14}$$

Topological state-3:

$$L_1\frac{di_{L1}}{dt} + V_{01} = 0 \tag{2.15}$$

$$L_2\frac{di_{L2}}{dt} + V_{02} = 0 \tag{2.16}$$

$$\frac{V_{01}}{R_1} - C_1\frac{dV_{01}}{dt} = i_{L1} \tag{2.17}$$

$$\frac{V_{02}}{R_2} - C_2\frac{dV_{02}}{dt} = i_{L2} \tag{2.18}$$

Equations (2.7) to (2.18) are written in the form of state space equations and the obtained state space matrices are stated below:

$$A_1 = \begin{pmatrix} 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C_1} & 0 & \frac{-1}{R_1C_1} & 0 \\ 0 & \frac{1}{C_2} & 0 & \frac{-1}{R_2C_2} \end{pmatrix}; \tag{2.19}$$

$$A_2 = \begin{pmatrix} 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C_1} & 0 & \frac{-1}{R_1C_1} & 0 \\ 0 & \frac{-1}{C_2} & 0 & \frac{1}{R_2C_2} \end{pmatrix}; \tag{2.20}$$

$$A_3 = \begin{pmatrix} 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{-1}{C_1} & 0 & \frac{1}{R_1C_1} & 0 \\ 0 & \frac{1}{C_1} & 0 & \frac{1}{R_2C_2} \end{pmatrix}; \tag{2.21}$$

$$B_1 = \begin{pmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \end{pmatrix}; B_2 = \begin{pmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{pmatrix}; B_3 = \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \end{pmatrix}; \tag{2.22}$$

$$C_1 = C_2 = C_3 = \begin{pmatrix} 0 & 0 & 1 & 1 \end{pmatrix} \tag{2.23}$$

To achieve state space matrices for the whole converter, equations (2.19) to (2.23) are multiplied by their respective topological duty cycles and are added respectively. Then, the state space matrices attained for the whole buck converter is given by:

$$A = \begin{pmatrix} 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C_1}(D_a) & 0 & \frac{-1}{R_1C_1}(D_a) & 0 \\ 0 & \frac{1}{C_2}(D_b) & 0 & \frac{-1}{R_2C_2}(D_b) \end{pmatrix} \tag{2.24}$$

$$B = \begin{pmatrix} \frac{1}{L_1}(D_x + D_y) \\ \frac{1}{L_2}(D_x) \\ 0 \\ 0 \end{pmatrix} \tag{2.25}$$

$$C = \begin{pmatrix} 0 & 0 & 1 & 1 \end{pmatrix} \tag{2.26}$$

In order to derive transfer function, we express these state space matrices in the form of state space equations. Which are stated below:

$$\frac{di_{L1}}{dt} = \frac{-(V_{o1})}{L_1} + \frac{(D_x + D_y)V_s}{L_1} \tag{2.27}$$

$$\frac{di_{L2}}{dt} = \frac{-(V_{o2})}{L_2} + \frac{(D_x)V_s}{L_2} \tag{2.28}$$

$$\frac{dV_{o1}}{dt} = \frac{(D_a)(i_{L1})}{C_1} + \frac{(D_a)V_{01}}{R_1C_1} \tag{2.29}$$

$$\frac{dV_{o2}}{dt} = \frac{(D_b)(i_{L2})}{C_2} + \frac{(D_b)V_{02}}{R_2C_2} \tag{2.30}$$

Applying Laplace transformation to the above equations (2.27) to (2.30) will yield the following equations:

$$Si_{L1}(s) = \frac{-(V_{o1}(s))}{L_1} + \frac{(D_x + D_y)V_s(s)}{L_1} \tag{2.31}$$

$$Si_{L2}(s) = \frac{-(V_{o2}(s))}{L_2} + \frac{(D_x)V_s(s)}{L_2} \tag{2.32}$$

$$SV_{o1}(s) = \frac{(D_a)(i_{L1}(s))}{C_1} + \frac{(D_a)V_{01}(s)}{R_1C_1} \tag{2.33}$$

$$SV_{o2}(s) = \frac{(D_b)(i_{L2}(s))}{C_2} + \frac{(D_b)V_{02}(s)}{R_2C_2} \tag{2.34}$$

On solving these above obtained Laplace equations we obtain transfer functions for the outputs $V_{01}$ and $V_{02}$ which are listed below in the following equations:

$$\frac{V_{01}(s)}{V_s(s)} = \frac{(D_x + D_y)(D_a)R_1}{S^2(R_1L_1C_1) + (L_1(D_a))S + (D_a)R_1} \tag{2.35}$$

$$\frac{V_{02}(s)}{V_s(s)} = \frac{(D_x)(D_b)R_2}{S^2(R_2L_2C_2) + (L_2(D_b))S + (D_b)R_2} \tag{2.36}$$

where $D_a$=$D_x$+$D_y$-$D_z$ and $D_b$=$D_x$-$D_y$-$D_z$

Since the frequency is equal to zero, thereby utilizing equations(2.1) to (2.6), the above transfer functions can be expressed as:

$$\frac{V_{01}(s)}{V_s(s)} = D_1 \tag{2.37}$$

$$\frac{V_{02}(s)}{V_s(s)} = 1 - D_2 \tag{2.38}$$

Where $D_1$ and $D_2$ represent the duty cycle of the switches $S_1$ and $S_2$.

## 2.3 Stability Conditions Derived through Routh Stability Criterion

Factorizing the numerator and denominator polynomials of the transfer function leads to the rise of zeros and poles respectively. As poles control the stability of the system [49], systems should be designed in such a way that poles obtained through the transfer functions always lie in the left hand side of an s-plane. So in order to locate the poles of a system on the s-plane, Routh stability criterion method is adopted. Where, characteristic equations are derived from the transfer functions and the resultant polynomials coefficients are utilized for calculation of an array. This stability criterion [49–51] states that, stability of the system depends on the number of sign changes that occur in the first column of an array, Where its conditions be listed as follows:

- No sign changes indicate the system to be absolutely stable.
- Number of sign changes indicate the number of poles that lie on the right hand side of s-plane, Which can be deduced that system is unstable.
- System can be marginally stable when there occurs a zero row in an array.

Using the equation (2.39), we derive the characteristic equations for both transfer functions that are represented below in the following equations (2.40) and (2.41):

$$1 + G(s) = 0 \tag{2.39}$$

$$(R_1L_1C_1)S^2 + (D_aL_1)S + (D_a)(D_x + D_y + 1)(R_1) = 0 \tag{2.40}$$

$$(R_2L_2C_2)S^2 + (D_bL_2)S + (D_b)(D_x + D_y + 1)(R_2) = 0 \tag{2.41}$$

Where G(s) is the transfer function.

Now Routh stability criterion is implemented, by ordering the coefficients as the initial two rows of an array. From these rows, the remaining two rows are calculated. Shown below is the array obtained for the characteristic equation (2.40).

| | | |
|---|---|---|
| $S^2$ | $R_1L_1C_1$ | $R_1(D_a)(D_x + D_y + 1)$ |
| $S^1$ | $D_a(L_1)$ | 0 |
| $S^0$ | $D_a(R_1)(D_x + D_y + 1)$ | |

Similarly array obtained for the characteristic equation (2.41) is,

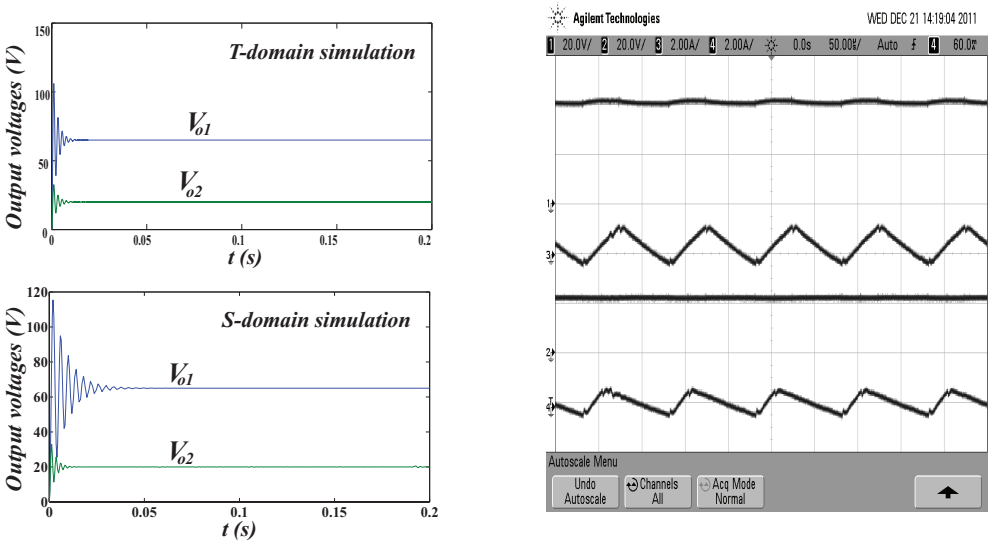
| | | |
|---|---|---|
| $S^2$ | $R_2L_2C_2$ | $R_2(D_a)(D_x + D_y + 1)$ |
| $S^1$ | $D_b(L_2)$ | 0 |
| $S^0$ | $D_b(R_2)(D_x + D_y + 1)$ | |

So from the array it can be observed that, resistance, inductance, capacitance and the duty cycles are of positive terms. Variables $D_a$ and $D_b$ should always remain positive for the converter to be operate in the stable region . As variables $D_a$ and $D_b$ depend on the topological duty cycles, PWM signals should be generated such that these variables are always greater than zero. We can also note that if $D_a$ and $D_b$ equals to zero, system can be considered as of marginally stable.

## 2.4 Simulation And Experimental Results

In order to validate the transfer function obtained from the small signal modeling derived in the chapter, simulations in t-domain and s-domain are performed. Fig. 2.3 (a) shows both outputs of the studied converter simulated dynamically in PSIM

(t-domain) and their equivalent in simulink (s-domain). Fig. 2.3 (b) shows the preliminary experimental results obtained when respective duty cycles $D_1$ and $D_2$ are considered to be 0.4 and 0.2. Here the inductor wave forms indicate the converter to be operating in the continuous conduction mode and the obtained output voltages are 40 V and 20 V.




(a) (b)

Fig. 2.3. (a) Simulated outcomes viewed in PSIM (t-domain) and simulink (s-domain), (b) Experimental results.

# 3. SINGLE INPUT TRIPLE OUTPUT DC-DC BUCK CONVERTER

## 3.1 Introduction

Applications of DC-DC converters include renewable energy systems [1], hybrid electric vehicles [5, 6], and uninterrupted power supplies [7, 8]. DC-DC converters can be made with both uni-directional and bi-directional power flow capabilities [1-4]. The uni-directional converter is made using a power switch, a power diode, and an *LC* filter [1-3, 14]. The bi-directional converter is achieved by removing the power diode and placing a power switch in parallel with the *LC* filter. Fig. 3.1 (a) shows that by replicating the bi-directional circuit three times, a bi-directional single-input three-output converter can be achieved. In [13], bi-directional DC-DC converters were shown to require smaller sized filters than that of a uni-directional converter. Faster dynamic response and lower device stress was also noted in the bi-directional converter [13]. In [12], a bi-directional DC-DC converter topology was proposed for use in applications that do not require magnetic components.

Applications such as communication systems and battery management systems require a DC-DC buck converter with multiple controlled outputs. In [17], a configuration was proposed that uses a single inductor for obtaining three controlled outputs. A three switch DC-DC buck converter topology was proposed in [18] that can be used in applications that require two controlled outputs. In this chapter, a novel single-input three-output DC-DC buck converter will be proposed. The proposed topology requires two less power switches than that of the conventional single-input three-output DC-DC buck converter. The differences of these converters are highlighted in Fig. 3.1.

### 3.2 Proposed Converter

The proposed topology consists of four power switches ($S_1$, $S_2$, $S_3$, and $S_4$) and three low pass filters ($L_1$-$C_1$, $L_2$-$C_2$, and $L_3$-$C_3$). The state of the switches is represented by binary variables, that is, $q_x = 0$ indicates that switch $S_x$ is OFF, and $q_x = 1$ indicates switch $S_x$ is ON, where $x$=1, 2, 3, and 4. Since there are four switches and two states for each switch, we attain 16 ways of operating the converter. Of these 16 states, only four are operational. All the other switching combinations should be avoided. Table 3.1 provides the topological states (TS) where TS-1, TS-2, TS-3, and TS-4 represent the operational states. It can be observed from Fig. 3.2 that:

For TS-1 ($q_1 = 0$, $q_2 = 1$, $q_3 = 1$, and $q_4 = 1$), the input energy is supplied to all the loads and inductors. This means inductors $L_1$, $L_2$, and $L_3$ will be charged (see Fig. 2(b)).

For TS-2 ($q_1 = 1$, $q_2 = 0$, $q_3 = 1$, and $q_4 = 1$), the input energy is provided to $R_1$, $L_1$, $R_2$, and $L_2$. Energy stored in inductor $L_3$ is dissipated. In Fig. 3.2(b), $i_{L3}$ flows in the closed path formed by switch $S_4$.

For TS-3 ($q_1 = 1$, $q_2 = 1$, $q_3 = 0$, and $q_4 = 1$), the input energy is provided to $R_1$ and $L_1$. Energy stored in inductors $L_2$ and $L_3$ is dissipated. This means the current $i_{L2}$ will be flowing in the closed path (see Fig. 3.2 (c)) formed by switch $S_3$ and $S_4$, and current $i_{L3}$ will be flowing in the closed path formed by switch $S_4$.

Finally, in TS-4 ($q_1 = 1$, $q_2 = 1$, $q_3 = 1$, and $q_4 = 0$), energy provided to all the inductors dissipates to their respective loads. Currents $i_{L1}$, $i_{L2}$, and $i_{L3}$ are discharged during this state (see Fig. 3.2 (d)).

### 3.3 Steady State Analysis

The proposed converter is assumed to be operating in continuous conduction mode with inductor waveforms presented in Fig. 3.3 (a). From the waveforms and topological states obtained in the previous sections, it can be deduced that variable $V_{R1}$ controls output voltage $V_{o1}$, variable $V_{R2}$ controls output voltage $V_{o2}$, and variable

Table 3.1.
Topological States

| | | | | |
|---|---|---|---|---|
| $q_1$ | 1 | 1 | 1 | 0 |
| $q_2$ | 1 | 1 | 0 | 1 |
| $q_3$ | 1 | 0 | 1 | 1 |
| $q_4$ | 0 | 1 | 1 | 1 |
| Topological states | TS-1 | TS-2 | TS-3 | TS-4 |

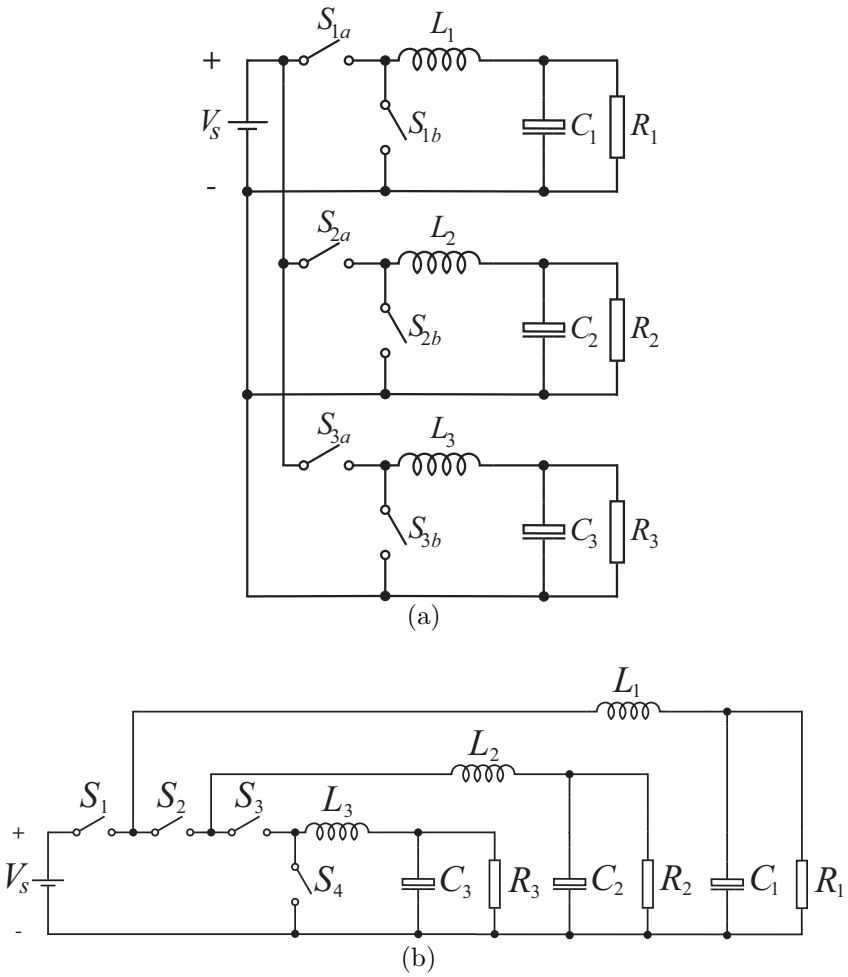



Fig. 3.1. Synchronous single-input multiple-output DC-DC converter for (a) Conventional topology, (b) Proposed topology.

$V_{R3}$ controls output voltage $V_{o3}$. Let $T_{on1}$, $T_{on2}$, and $T_{on3}$ be the time periods during which respective PWM generators 1, 2, and 3 are producing logic "1" at their output. Since the average inductor voltage is zero, the following equations can be obtained:

$$(V_s - V_{01})T_{on1} = V_{01}(T_s - T_{on1}) \tag{3.1}$$

$$(V_s - V_{02})(T_s - T_{on2}) = V_{02}T_{on2} \tag{3.2}$$

$$(V_s - V_{03})(T_s - T_{on3}) = V_{03}T_{on3} \tag{3.3}$$

From the above equations, the output voltages can be derived as a function of their duty cycles and supply voltage. The output voltages are represented in the below equations

$$V_{o1} = (D_{gen1})V_s \tag{3.4}$$

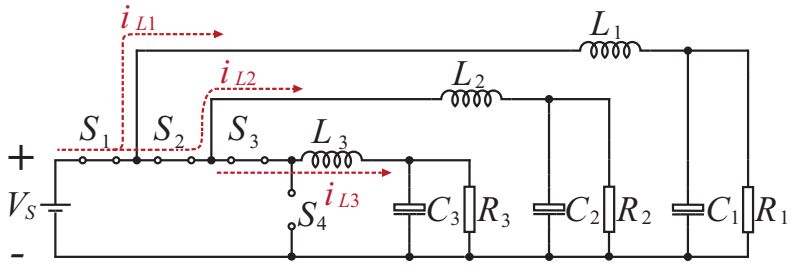
$$V_{o2} = (1 - D_{gen2})V_s \tag{3.5}$$

$$V_{o3} = (1 - D_{gen3})V_s \tag{3.6}$$

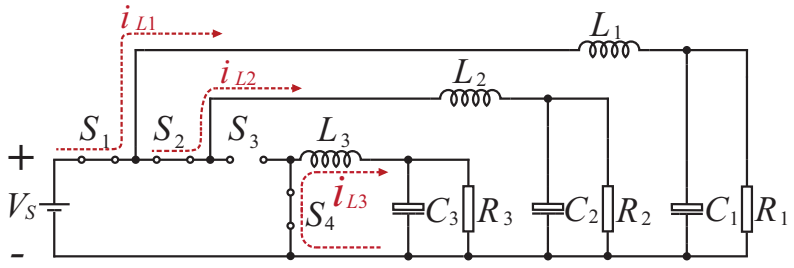
where $D_{gen1}$, $D_{gen2}$, and $D_{gen3}$ represent the duty cycles.

### 3.4 Independent Output Voltage Generation

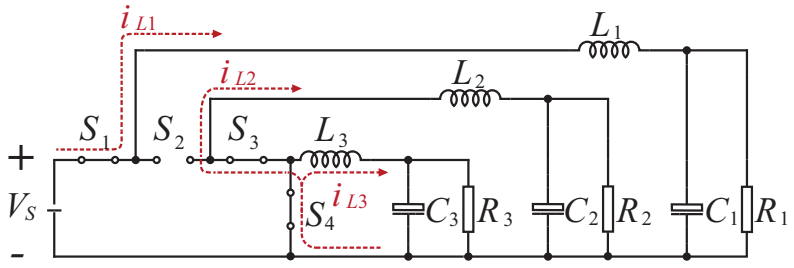
The duty cycle of switch $S_1$ can be varied from a minimum value of 0 to a maximum value of 1. Assuming the duty cycle for switch $S_1$ is $D_1 = 3/4$, the output voltage on load 1 would be 75% of the input voltage. The duty cycle of switch $S_2$ can be varied from 0 to $D_1$. Similarly, the duty cycle of the switch $S_3$ can be varied from 0 to $D_2$. As a result, the output voltage across load 1 is always higher than the voltage across load 2, and the output voltage across load 2 is always higher than the output voltage across load 3. In conventional converters, the output voltage at every load can be varied by changing their respective duty cycles from 0 to 1. This means $0 < D_1 < 1$, $0 < D_2 < 1$, and $0 < D_3 < 1$.



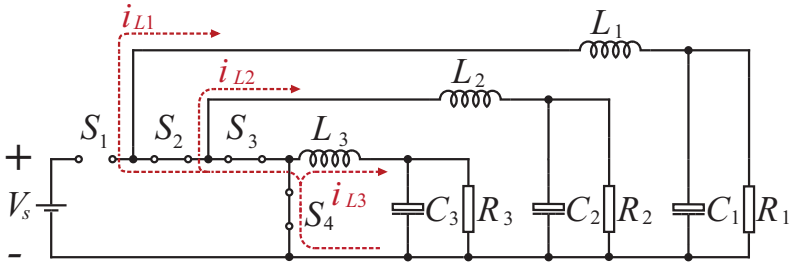

(a)




(b)




(c)




(d)

Fig. 3.2. Modes of operation: (a) TS-1, (b) TS-2, (c) TS-3, and (d) TS-4.

### 3.4.1 Pulse Width Modulation

The four switches discussed in the previous section are operated using pulse width modulation(PWM) technique. This modulation approach deals with a comparison of reference voltages $V_{R1}^*$, $V_{R2}^*$, and $V_{R3}^*$ with a saw-tooth wave form. The output of this comparison goes through a logic circuit which dictates the state of the switches. These reference voltages will control the output voltages across $R_1$, $R_2$, and $R_3$. Note that the output of the first PWM generator will be the difference between the saw-tooth waveform and $V_{R1}^*$. Similarly, the output of the second and third PWM generator will be obtained with respect to $V_{R2}^*$, and $V_{R3}^*$ respectively.

The PWM logic circuit implementation shown in Fig. 3.3 (d) is used for controlling the duty cycle of the switches. This circuit is built, based on few conclusion that were developed from the operation of the converter described during its corresponding topological state.

The charging of inductor $L_1$ is entirely dependent on switch $S_1$. Hence, the first PWM generator can be directly connected to switch $S_1$ to control the output voltages $V_{01}$ or the state of inductor $L_1$.

During the topological state (TS-4), switch $S_2$ is "ON", at the same time, inductor $L_2$ is discharging during this period of time. This means that, the charging and discharging of the inductor $L_2$ is not dependent on the state of the switch $S_2$. Note that, switch $S_2$ should be operated in such a way that topological states TS-1 and TS-2 remain for an interval that can be defined by the second PWM generator. In addition, switch $S_2$ should be controlled in such a way that prohibited states are avoided. These requirements are achieved by using a two input "OR" gate and a "NOT" gate shown in Fig. 3.3 (c).

By Similar observation, switch $S_3$ should be operated in such a way that topological state TS-1 remains for an interval of time that is defined by third PWM generator. Switch $S_3$ should also be controlled in such a way that, it stays "ON" when either of switches $S_1$ or $S_2$ turns "OFF". These requirements can be satisfied by using a three

input "OR" gate in which, the output of third PWM generator and the inverse of the first and second generators are connected. Switch $S_4$ is defined by the state of the switches $S_1$, $S_2$, and $S_3$. This means that the function of switch $S_4$ in the circuitry is to avoid the prohibited states. This control of the switch can be achieved by using a "NAND" gate.

Fig. 3.3 (b) shows the gating signals that are obtained for switches $S_1$, $S_2$, $S_3$, and $S_4$ respectively.

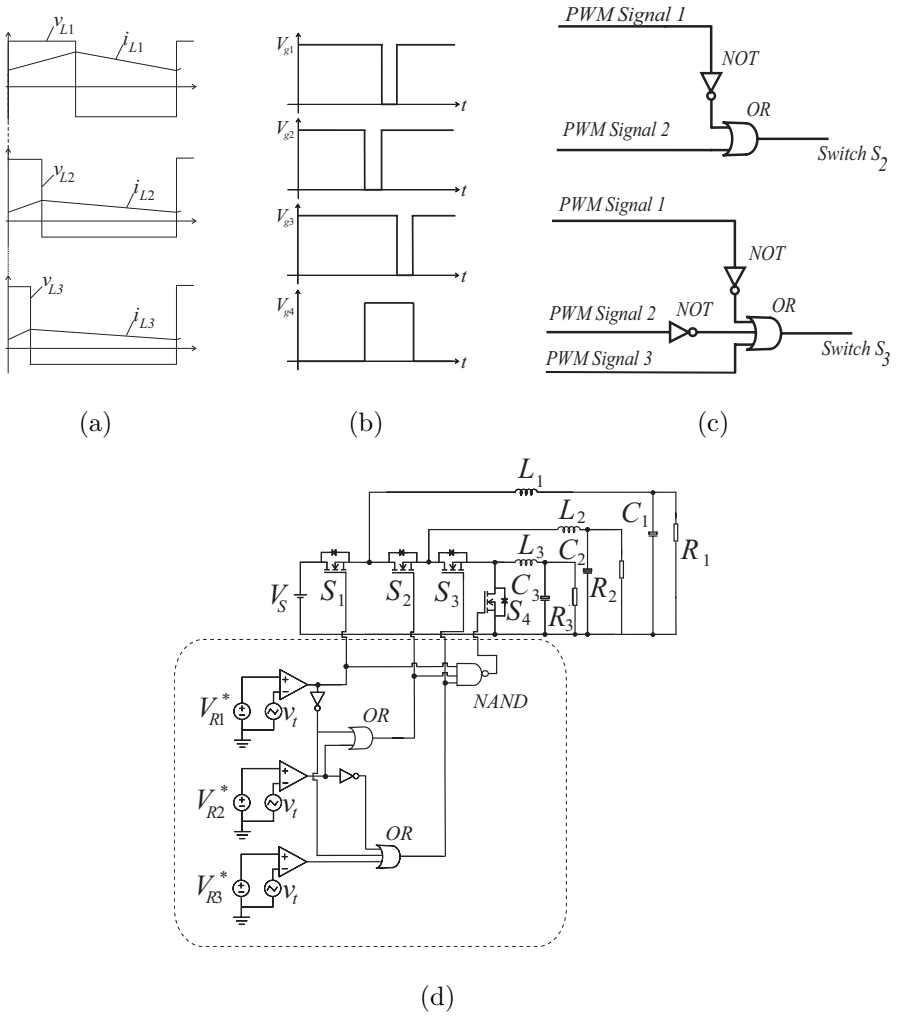



Fig. 3.3. (a) Voltage and current waveforms for $L_1$, $L_2$ and $L_3$, (b) Gating signal for switches $S_1$, $S_2$, $S_3$, and $S_4$ respectively, (c) Logic circuit implementation, (d) PWM implementation for the proposed topology,.

### 3.5 Small Signal Analysis

In the case of designing a controller or assessing the performance for a converter, the linearization techniques discussed in [43] can be used. In order to have a clear understanding on the dynamics of the novel configuration, small signal analysis is performed and transfer functions are derived. Following the procedure outlined in [48], Kirchoff's laws are applied on the topological states, and their corresponding equations are as follows:

Topological state-1:

$$L_1\frac{di_{L1}}{dt} + V_{01} = V_s \tag{3.7}$$

$$L_2\frac{di_{L2}}{dt} + V_{02} = V_s \tag{3.8}$$

$$L_3\frac{di_{L3}}{dt} + V_{03} = V_s \tag{3.9}$$

$$C_1\frac{dV_{01}}{dt} + \frac{V_{01}}{R_1} = i_{L1} \tag{3.10}$$

$$C_2\frac{dV_{02}}{dt} + \frac{V_{02}}{R_2} = i_{L2} \tag{3.11}$$

$$C_3\frac{dV_{03}}{dt} + \frac{V_{03}}{R_3} = i_{L3} \tag{3.12}$$

Topological state-2:

$$L_1\frac{di_{L1}}{dt} + V_{01} = V_s \tag{3.13}$$

$$L_2\frac{di_{L2}}{dt} + V_{02} = V_s \tag{3.14}$$

$$L_3\frac{di_{L3}}{dt} + V_{03} = 0 \tag{3.15}$$

$$C_1\frac{dV_{01}}{dt} + \frac{V_{01}}{R_1} = i_{L1} \tag{3.16}$$

$$C_2\frac{dV_{02}}{dt} + \frac{V_{02}}{R_2} = i_{L2} \tag{3.17}$$

$$\frac{V_{03}}{R_3} - C_3\frac{dV_{03}}{dt} = i_{L3} \tag{3.18}$$

Topological state-3:

$$L_1\frac{di_{L1}}{dt} + V_{01} = V_s \tag{3.19}$$

$$L_2\frac{di_{L2}}{dt} + V_{02} = 0 \tag{3.20}$$

$$L_3\frac{di_{L3}}{dt} + V_{03} = 0 \tag{3.21}$$

$$C_1\frac{dV_{01}}{dt} + \frac{V_{01}}{R_1} = i_{L1} \tag{3.22}$$

$$\frac{V_{02}}{R_2} - C_2\frac{dV_{02}}{dt} = i_{L2} \tag{3.23}$$

$$\frac{V_{03}}{R_3} - C_3\frac{dV_{03}}{dt} = i_{L3} \tag{3.24}$$

Topological state-4:

$$L_1\frac{di_{L1}}{dt} + V_{01} = 0 \tag{3.25}$$

$$L_2\frac{di_{L2}}{dt} + V_{02} = 0 \tag{3.26}$$

$$L_3\frac{di_{L3}}{dt} + V_{03} = 0 \tag{3.27}$$

$$\frac{V_{01}}{R_1} - C_1\frac{dV_{01}}{dt} = i_{L1} \tag{3.28}$$

$$\frac{V_{02}}{R_2} - C_2\frac{dV_{02}}{dt} = i_{L2} \tag{3.29}$$

$$\frac{V_{03}}{R_3} - C_3\frac{dV_{03}}{dt} = i_{L3} \tag{3.30}$$

The above equations are expressed in the form of state space equations and their resultant state space matrices are represented below. Here, $A_1$, $B_1$, and $C_1$ are the state space matrices which are obtained for the topological state-1. Similarly, the corresponding state space equations for TS-2, TS-3, and TS-4 were also derived and are as follows:

$$B_1 = \begin{pmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ \frac{1}{L_3} \\ 0 \\ 0 \\ 0 \end{pmatrix}; B_2 = \begin{pmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix}; B_3 = \begin{pmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix}; B_4 = \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix}; \tag{3.31}$$

$$C_1 = C_2 = C_3 = C_4 = \begin{pmatrix} 0 & 0 & 0 & 1 & 1 & 1 \end{pmatrix}; \tag{3.32}$$

$$A_1 = \begin{pmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_3} \\ \frac{1}{C_1} & 0 & 0 & \frac{-1}{R_1 C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 & \frac{-1}{R_2 C_2} & 0 \\ 0 & 0 & \frac{1}{C_3} & 0 & 0 & \frac{-1}{R_3 C_3} \end{pmatrix}; \tag{3.33}$$

$$A_2 = \begin{pmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_3} \\ \frac{1}{C_1} & 0 & 0 & \frac{-1}{R_1 C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 & \frac{1}{R_2 C_2} & 0 \\ 0 & \frac{-1}{C_3} & 0 & 0 & 0 & \frac{1}{R_3 C_3} \end{pmatrix}; \tag{3.34}$$

$$A_3 = \begin{pmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_3} \\ \frac{1}{C_1} & 0 & 0 & \frac{1}{R_1 C_1} & 0 & 0 \\ 0 & \frac{-1}{C_2} & 0 & 0 & \frac{1}{R_2 C_2} & 0 \\ 0 & 0 & \frac{-1}{C_3} & 0 & 0 & \frac{1}{R_3 C_3} \end{pmatrix}; \tag{3.35}$$

$$A_4 = \begin{pmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_3} \\ \frac{-1}{C_1} & 0 & 0 & \frac{1}{R_1 C_1} & 0 & 0 \\ 0 & \frac{-1}{C_2} & 0 & 0 & \frac{1}{R_2 C_2} & 0 \\ 0 & 0 & \frac{-1}{C_3} & 0 & 0 & \frac{1}{R_3 C_3} \end{pmatrix}; \tag{3.36}$$

From the topological states that were depicted in the Fig. 3.2, it is good to mention that the converter operates in these states for a definite period of time. If $D_a$, $D_b$, $D_c$, and $D_d$ are considered as duty cycles for the respective topologies TS-1,

TS-2, TS-3, and TS-4. State space matrices for the whole converter are derived by adding the resultant matrices, which are obtained by multiplying the above state space matrices (3.31) to (3.36) with their corresponding topological duty cycles. Equations represented below are the state space equations for the proposed single input triple output DC-DC buck converter.

$$\frac{di_{L1}}{dt} = \frac{-(V_{o1})}{L_1} + \frac{(T_1+T_2+T_3)V_s}{L_1} \tag{3.37}$$

$$\frac{di_{L2}}{dt} = \frac{-(V_{o2})}{L_2} + \frac{(T_1+T_2)V_s}{L_2} \tag{3.38}$$

$$\frac{di_{L3}}{dt} = \frac{-(V_{o3})}{L_3} + \frac{(T_1)V_s}{L_3} \tag{3.39}$$

$$\frac{dV_{o1}}{dt} = \frac{(T_1+T_2+T_3-T_4)(i_{L1})}{C_1} + \frac{(T_1+T_2+T_3-T_4)V_{01}}{R_1C_1} \tag{3.40}$$

$$\frac{dV_{o2}}{dt} = \frac{(T_1+T_2-T_3-T_4)(i_{L2})}{C_1} + \frac{(T_1+T_2-T_3-T_4)V_{02}}{R_2C_2} \tag{3.41}$$

$$\frac{dV_{o3}}{dt} = \frac{(T_1-T_2-T_3-T_4)(i_{L3})}{C_1} + \frac{(T_1-T_2-T_3-T_4)V_{03}}{R_3C_3} \tag{3.42}$$

Laplace transformation is applied on the converter's state space equations, and transfer functions are derived. The obtained transfer functions are:

$$\frac{V_{01}(s)}{V_s(s)} = \frac{(D_a+D_b+D_c)(D_x)R_1}{S^2(R_1L_1C_1)+(L_1(D_x))S+(D_x)R_1} \tag{3.43}$$

$$\frac{V_{02}(s)}{V_s(s)} = \frac{(D_a+D_b)(D_y)R_2}{S^2(R_2L_2C_2)+(L_2(D_y))S+(D_y)R_2} \tag{3.44}$$

$$\frac{V_{03}(s)}{V_s(s)} = \frac{(D_a)(D_z)R_3}{S^2(R_3L_3C_3)+(L_3(D_z))S+(D_z)R_3} \tag{3.45}$$

where $D_x$=($D_a$+$D_b$+$D_c$-$D_d$), $D_y$=($D_a$+$D_b$-$D_c$-$D_d$) and $D_z$=($D_a$-$D_b$-$D_c$-$D_d$).

In order to express the output variables with respect to input and control parameters, topological duty cycles $D_a$, $D_b$, $D_c$, and $D_d$ are related with the duty cycles generated by PWM generators 1, 2, and 3. Resultant expressions are listed in the following equations.

$$D_a + D_b + D_c = D_{gen1} \tag{3.46}$$

$$D_a + D_b = D_{gen2} \tag{3.47}$$

$$D_a = D_{gen3} \tag{3.48}$$

Since the state space frequency of DC-DC converter is zero, by Substituting the above equations(3.46) to (3.48) in (3.43) to (3.45), the transfer functions can be minimized into the following expressions.

$$\frac{V_{01}(s)}{V_s(s)} = D_{gen1} \tag{3.49}$$

$$\frac{V_{02}(s)}{V_s(s)} = D_{gen2} \tag{3.50}$$

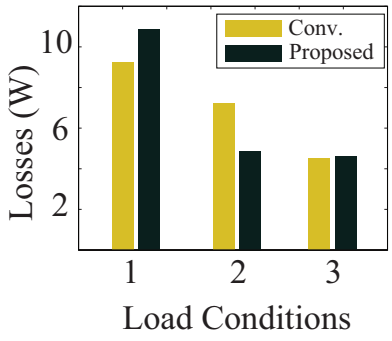
$$\frac{V_{03}(s)}{V_s(s)} = D_{gen3} \tag{3.51}$$

# 4. SIMULATION AND EXPERIMENTAL RESULTS

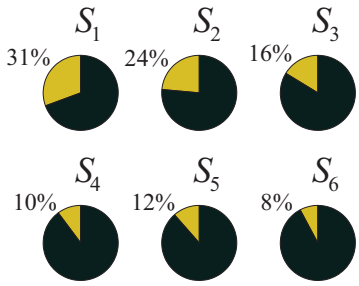
In this chapter, simulation and experimental results carried out on the single input triple output DC-DC buck converter will be presented in detail.

## 4.1 Comparison of Switching Losses among the Topologies

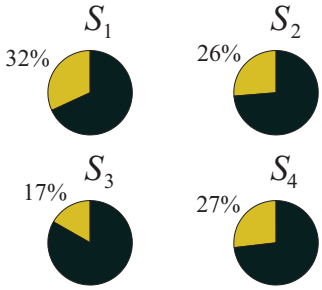
This section discusses the advantages and disadvantages of the proposed topology when it is compared with the traditional configuration. PSIM software offers thermal modules that are used to calculate the losses, specifically the one used for this comparison was for the IRFP 460 MOSFET. Fig. 4.1 (a) shows the total semiconductor losses for both topologies. It can be seen that under some load conditions, the proposed topology offers semiconductor losses that are better, worse, or even the same as for a conventional one. Even though it does not always offer better efficiency, the proposed circuit does offer better power loss distribution among the switches in every case, which can be seen by comparing Fig. 4.1 (b) and 4.1 (c). The proposed and conventional circuit were put under the exact same conditions during the tests, that is $Vs = 300V$, $L_1 = L_2 = L_3 = 0.001$H, and $C_1 = C_2 = C_3 = 0.00012$F. Under load conditions of $R_1 = R_2 = R_3 = 100\Omega$, the conventional topology had 97% efficiency while the proposed converter had 96% efficiency. Under load conditions $R_1 = 3000\Omega$, $R_2 = 2000\Omega$, and $R_3 = 50\Omega$, the conventional topology had an efficiency of 91% and the proposed topology had an efficiency of 93%. Both topologies operated at 94% efficiency under load conditions $R_1 = 3000\Omega$ and $R_2 = R_3 = 2000\Omega$.




(a)




(b)




(c)

Fig. 4.1. (a) Semiconductor losses under different load conditions, (b) Traditional semiconductor loss distribution, (c) Proposed semiconductor loss distribution.

## 4.2 Simulation and Experimental Results

Considering $V_s = 100V$, $L_1 = L_2 = L_3 = 0.06$mH, $C_1 = C_2 = C_3 = 0.0022$F, $R_1 = R_2 = R_3 = 100, \Omega$ $V_{R1}$=55V, $V_{R2}$=30V, and $V_{R3}$=15V as the parameters, the

simulation of the proposed topology is analyzed using PSIM. A proof of concept prototype was built in the laboratory using a dsPIC (dsPICJ64MC802), 4 IGBTs (BSM75GB60DLC), and their drivers (2BB0108T2Ax-17). dsPIC is a micro controller programmed in such a way that the desired gating signals are generated for every switch. PWM signals generated from the dsPIC are shown in the Fig. B.1. Some of the waveforms obtained are presented in this section.

Simulation results obtained for the gating signals, output voltages, and regulating the output voltages for any change in the input voltages are shown in Fig. 4.2 and Fig. 4.3. A dead time of 200 nanoseconds was also implemented using the dsPIC. Dead time generated between PWM signals 2 and 3 is shown in Fig. B.2.

Experimental results and their corresponding simulation results achieved are shown in the Fig. 4.4, Fig. 4.5, and Fig. 4.6. Inductor current $I_{L1}$ has been shown in all the experimental results to show that experiments are performed on the proposed topology. Fig. 4.4(a) shows the currents and voltages across inductor $L_1$ and the output voltage $V_{01}$. Fig. 4.4(b) shows their corresponding simulation results. Fig. 4.5(a), shows the current $I_{L1}$ and voltages across inductor $L_2$ and at the load $R_2$. Fig. 4.5(b) shows their corresponding simulation results. Fig. 4.6(a), shows the current $I_{L1}$ and voltages across inductor $L_3$ and at the load $R_3$. Fig. 4.6(b) shows their corresponding simulation results. It can be seen that the output voltages, inductor current, and inductor voltages all match the waveforms obtained in the experimental setup.

When taking the ripple content in to account, the comparison of the experimental and the simulated results showed that the experimental results yielded a higher value. This is due to the fact that the series resistance added by the capacitor is neglected during the simulation.

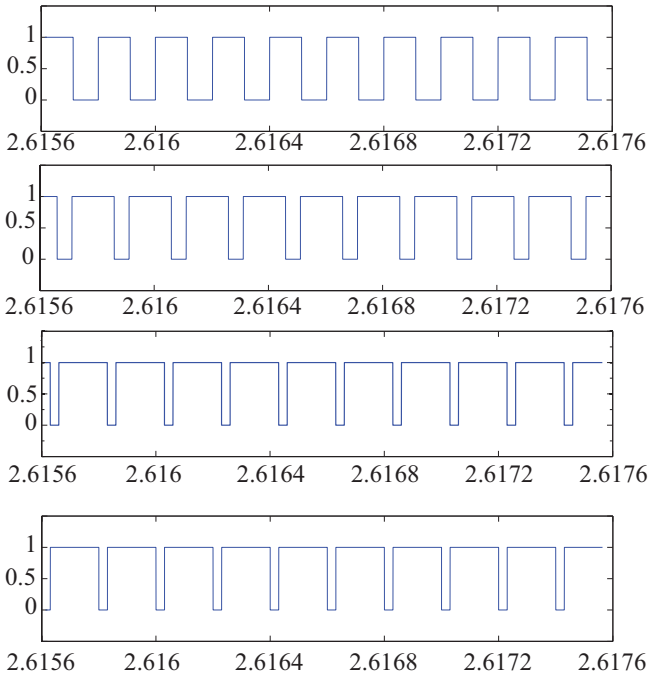



Fig. 4.2. Gating signals viewed in PSIM

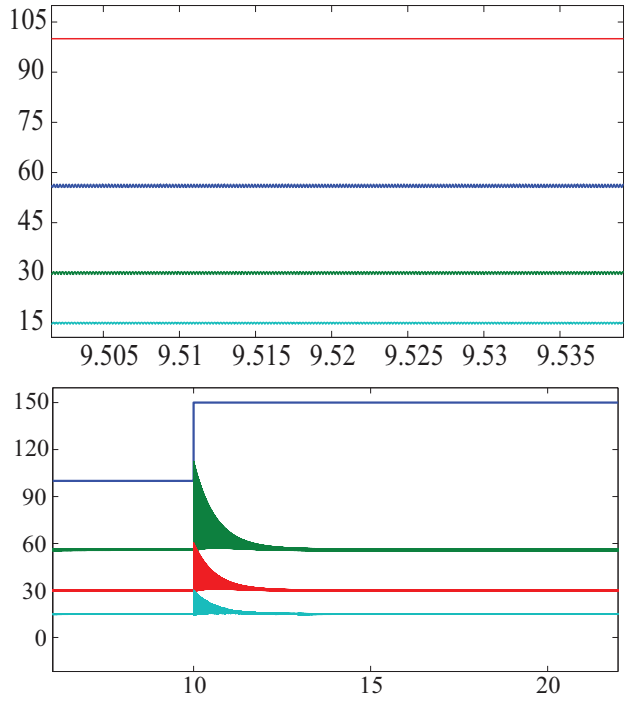
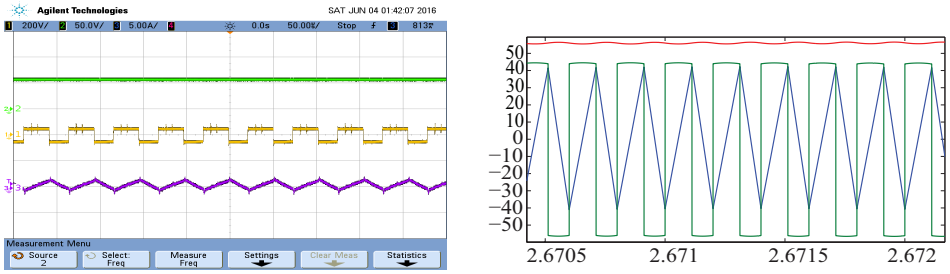
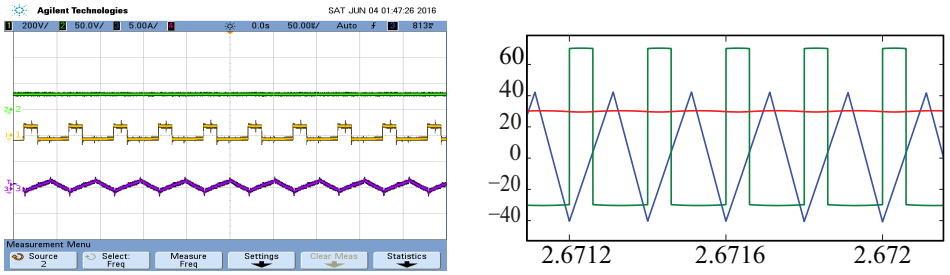



Fig. 4.3. PSIM simulation Results: Input and output voltages, Regulated output voltages with respect to change in the input voltage.



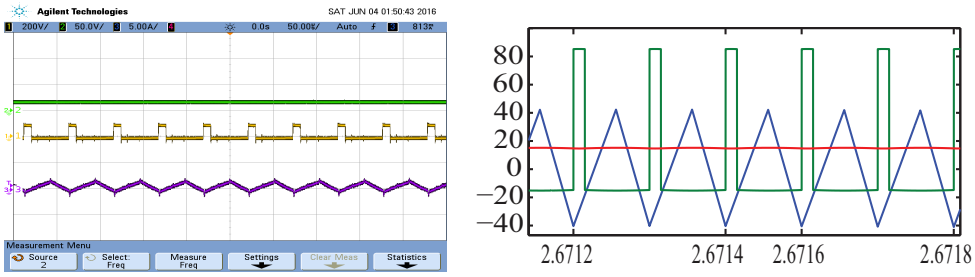

(a) (b)

Fig. 4.4. Comparison of output voltage $V_{01}$, inductor voltage $V_{L1}$ and inductor current $I_{L1}$: (a) Experimental results, (b) Simulation results.




(a) (b)

Fig. 4.5. Comparison of output voltage $V_{02}$, inductor voltage $V_{L2}$ and inductor current $I_{L1}$: (a) Experimental results, (b) Simulation results.




(a) (b)

Fig. 4.6. Comparison of output voltage $V_{03}$, inductor voltage $V_{L3}$ and inductor current $I_{L1}$: (a) Experimental results, (b) Simulation results.

# 5. CONCLUSION AND FUTURE EXTENSIONS

## 5.1 Conclusion

New converter topology is proposed where the converter utilizes the single input to generate three output voltages. The converter topology, operational modes, modulation techniques, and design specification were presented. Similar analysis which was carried out in the chapter 2 is performed on the topology proposed in chapter 3 for determining the transfer function of single input triple output DC-DC converter. Simulation and experimental results were presented in the following chapter.

At the end, by comparing the simulation and experimental results, following observations are made: Results obtained through the experiments carried out in the laboratory are identical to those of simulation results, which verifies the analysis performed. Proposed converter has a draw back of having power switches with higher current ratings. But, the advantages of the proposed configuration include reduction of the number of driver circuits, and better power loss distribution among the switches.

## 5.2 Future Extensions

Since the converter configuration posses several advantages and has an innumerable applications, introducing this product into the market would be a game changer. So to get implemented, some additional analysis has to be done in this area. Some of them are listed below,

- Testing the operating limits
- Developing the non-linear control strategies

- Thermal analysis
- Analysis on Electro Magnetic Interference (EMI)
- Tests to evaluate the life expectancy of the equipment

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# APPENDICES

# A. INTRODUCTION

As chapter 3 introduces a novel topology in the area of single input multiple output DC-DC buck converters. At first, this circuit configuration is simulated in PSIM and to validate the simulation results obtained from the PSIM, a prototype was created as shown in the Fig. A.1.

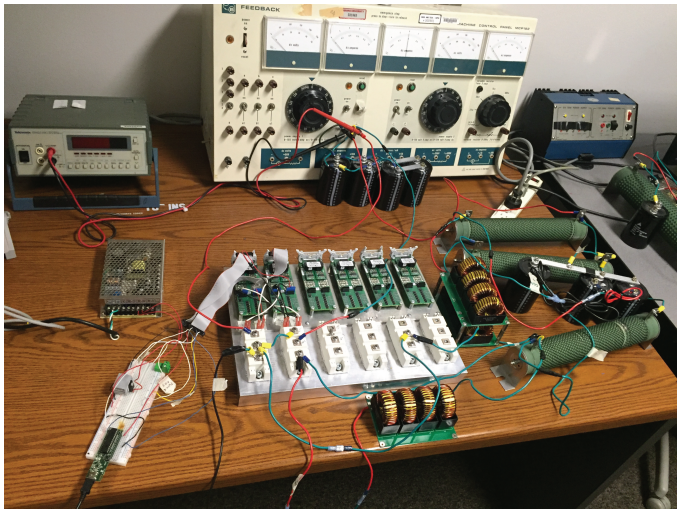

Fig. A.1. Prototype of single input triple output DC-DC buck converter

Fig. A.1 represents the experimental setup, in which the switching module is placed at the center. The switching module in turn has 6 IGBT modules and 6 gate driver circuits, mounted on a heat sink. Since each IGBT module accommodates 2 IGBT's, two driver circuits and IGBT modules on the left are employed in the prototype. Also a dsPIC and voltage regulator were set on a bread board. In addition to these, the voltage regulator also has a heat sink attached to it, to dissipate the heat generated. Both the switching module and outputs available from the bread board are connected together using connecting wires. On the right side of the switching module, three sets of resistors, capacitors and inductors are placed. Here resistors

are considered as loads and, the inductors and capacitors are considered as the LC filters. Input power supply to the entire setup is provided using the Machine Control Panel (MCP 182), which can generate a voltage ranging from 0-135 volts and current ranging from 0-5 amps. MCP 182 is a huge device that is placed behind the switching module in the Fig. A.1. On the left side of machine control panel, Tektronics DM 2510G is placed, which displays the voltage being applied to the converter.

Components which were used while building the prototype and their functions are listed below:

DSPIC J64MC802 - DSPIC used for generating the PWM signals. It is programmed in such a way that it generates desired PWM signals of 20KHZ with an added dead time.

Infineon BSM75GB60DLC - an IGBT module employed for the switches $S_1$, $S_2$, $S_3$ and $S_4$. Where, each module accommodates 2 IGBT's.

CONCEPT 2SC0108T2A0-17 - Gate driver circuit, which acts as an interface between the DSPIC and the IGBT modules.

7815 A JRC ME011A - A voltage regulator to supply the input power to the driver circuit.

Tektronics DM 2510G - utilized for measuring the input voltage supplied to the converter.

DSO7014B - Digital Storage Oscilloscope for capturing the output dynamics of the converter.

# B. PROGRAMMING DSPIC J64MC802

In this section, important lines in code which are responsible for programming the DSPIC are dealt. Initially, library files and an oscillator is set up. Later, ports where the outputs are to be observed are initialized. At the end, following lines of code were written in order to generate the 4 PWM signals with an added dead time of 200 nano seconds.

```
while(1){
if (x==ti)
{
x=0;
}
/* First PWM signal*/
if(x>=28)   /if(x&lt;=(0.55*ti))/*if(x<=(0.3*ti) && x>=(0.55*ti))*/
{PORTBbits.RB5=1 ;}        /*port RB5 is set high*/
else
{PORTBbits.RB5=0 ;}       /* port RB5 set low*/
/* Second PWM signal*/
if(x<=15 || x>28)    /*if(x<=(0.3*ti) && x>=(0.55*ti))*/
{PORTBbits.RB7=1 ;}
else
{PORTBbits.RB7=0 ;}
/* Third PWM signal*/
if(x<=8 || x>15)  /*if(x<=(0.16*ti) && x>(0.3*ti)) */
{PORTBbits.RB4=1 ;}
else
```

```
{PORTBbits.RB4=0 ;}
/* fourth PWM signal*/
if(x>8 && x<49)
{PORTBbits.RB6=1 ;}
else
{PORTBbits.RB6=0 ;}
x=x+1;
}
}
```

Here continuous signal is generated using “while” statement that creates an infinite loop. “ti” which is equal to 50, is a variable that acts as a counter. Variable “x” gets incremented by one for every iteration. The main function of the counter is to reset the variable “x” whenever it reaches the value 50. Ports RB4, RB5, RB6 and RB7 are the output ports, These ports go high when they are set to ‘1’ and they go low when they are set to ‘0’. If-else statement has been utilized for giving the ports their corresponding values. Conditions were written based on the output voltages that are to be obtained near the load.

Following are the results observed near the DSPIC, Fig. B.1, shows the gating signals generated and Fig. B.2, shows the dead time observed between the PWM signals 2 and 3.


Fig. B.1. PWM signals generated from the DSPIC 33F64FJMC802

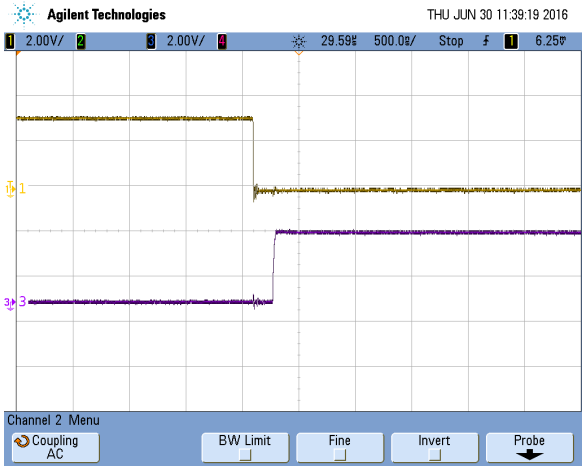


Fig. B.2. Dead time generated between the ports RB5 and RB7